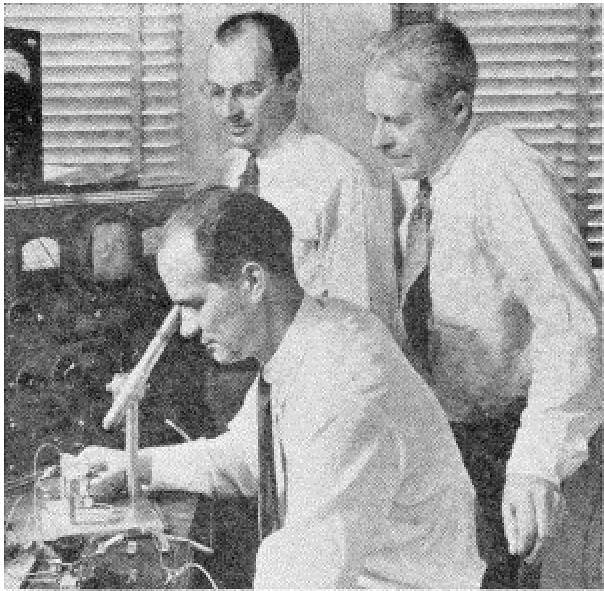
Logic Families

Dr. Basem Elhalawany

A bit of history

- The first transistors were fabricated in 1947 at Bell Laboratories (Bell Labs) by Brattain with Bardeen providing the theoretical background and Shockley managed the activity.
  - The trio received a Nobel Prize in Physics for their work in 1956.
    - The transistor was called a point-contact transistor and was a type of bipolar junction transistor (BJT).



A bit more history

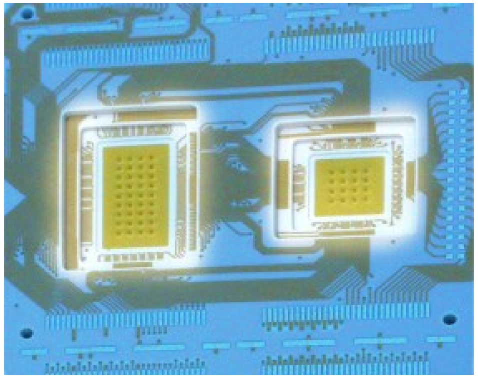
- The theory on field effect transistors (FETs) was developed much earlier than our understanding of BJTs
  - First patent on FETs dates from 1925
    - Julius Edgar Lilienfeld, an Austro-Hungarian physicist
- However, the quality of the semiconductor and the oxide materials were barriers to developing good working devices.
  - The first FET was not invented until 1959
    - Dawon Kahng and Martin M. (John) Atalla of Bell Labs

Integrated Circuits

- Integrated circuits (ICs) are chips, pieces of semiconductor material, that contain all of the transistors, resistors, and capacitors necessary to create a digital circuit or system.
  - The first ICs were fabricated using Ge BJTs in 1958.
    - Jack Kirby of Texas Instruments, Nobel Prize in 2000
    - Robert Noyes of Fairchild Semiconductors fabricated the first Si ICs in 1959.

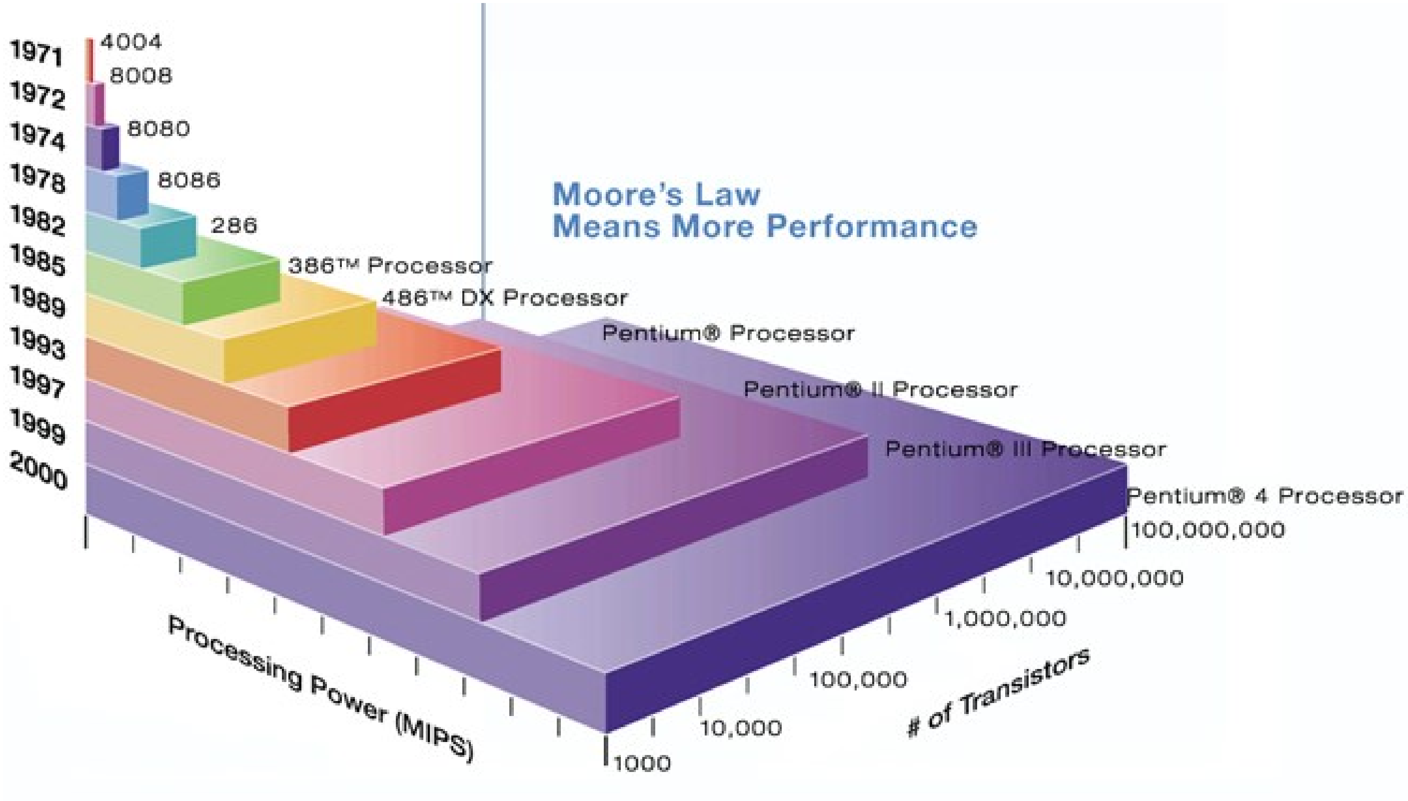
Integration Levels

– SSI Small scale integration	12 gates/chip
– MSI Medium scale integration	100 gates/chip
– LSI Large scale integration	1K gates/chip
– VLSI Very large scale integration	10K gates/chip
– ULSI Ultra large scale integration	100K gates/chip



Moore's law

- A prediction made by Moore (a co-founder of Intel) in 1965: "… a number of transistors to double every 2 years."



Logic Families

- Logic families are sets of chips that may implement different logical functions, but use the same type of transistors and voltage levels for logical levels and for the power supplies.
- These families vary by speed, power consumption, cost, voltage & current levels

- IC digital logic families
  - DL (Diode- logic)
  - DTL（Diode-transistor logic）
  - RTL（Resistor-transistor logic）
  - TTL（Transistor -transistor logic）
  - ECL（Emitter-coupled logic）
  - MOS（Metal-oxide semiconductor）
  - CMOS (Complementary Metal-oxide semiconductor）

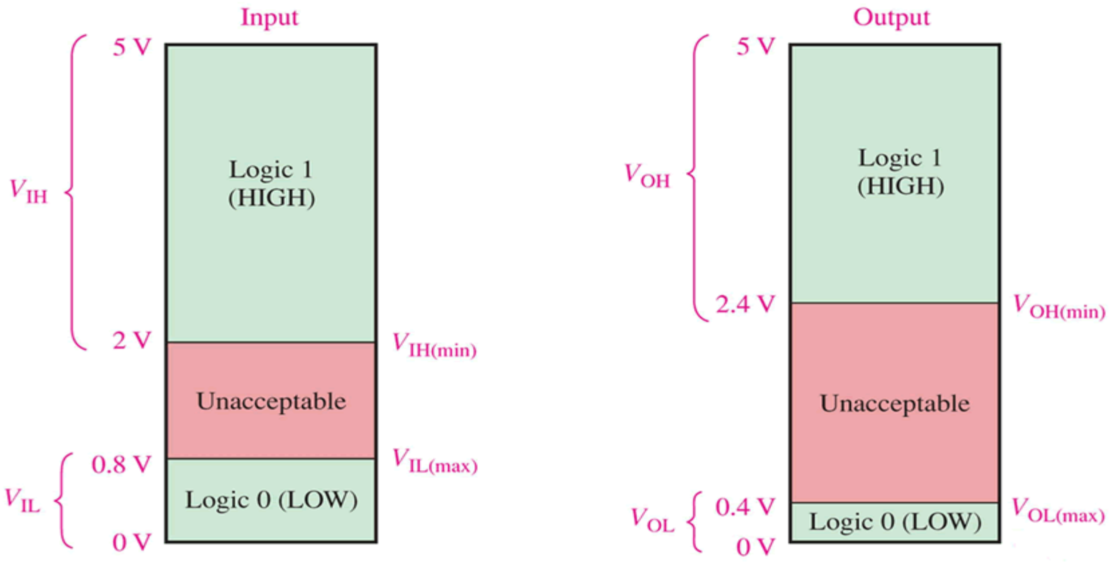
• Voltage Parameters:

Digital IC Terminology

- V_{IH}(min): high-level input voltage, the minimum voltage level required for a logic 1 at an *input*.
- V_{IL}(max): low-level input voltage
- V_{OH}(min): high-level output voltage
- V_{OL}(max): low-level output voltage

- For proper operation the input voltage levels to a logic must be kept outside the indeterminate range.
- Lower than V_{IL}(max) and higher than V_{IH}(min).

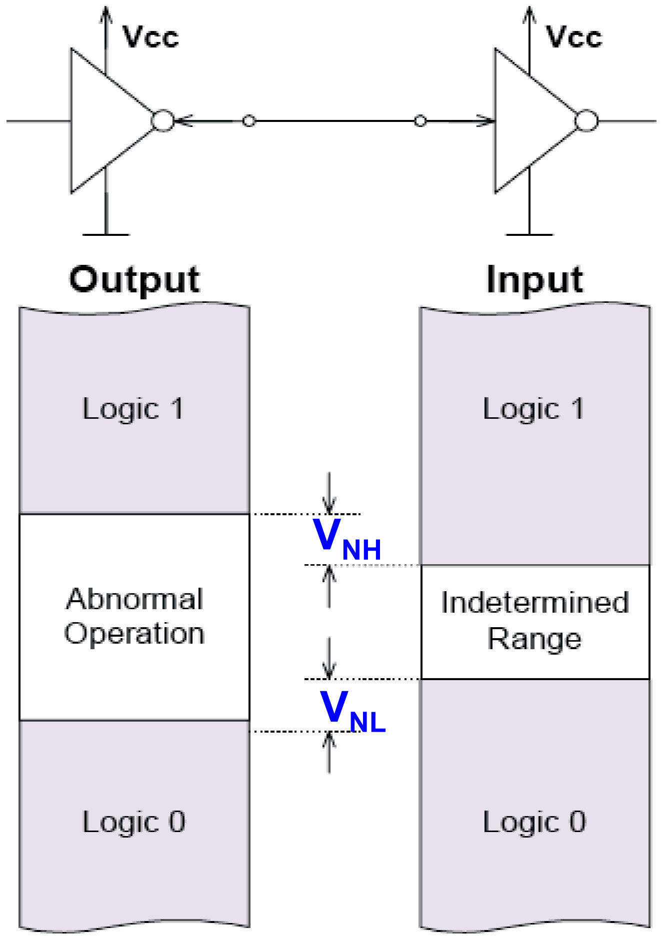
For TTL



Noise Margin

Digital IC Terminology

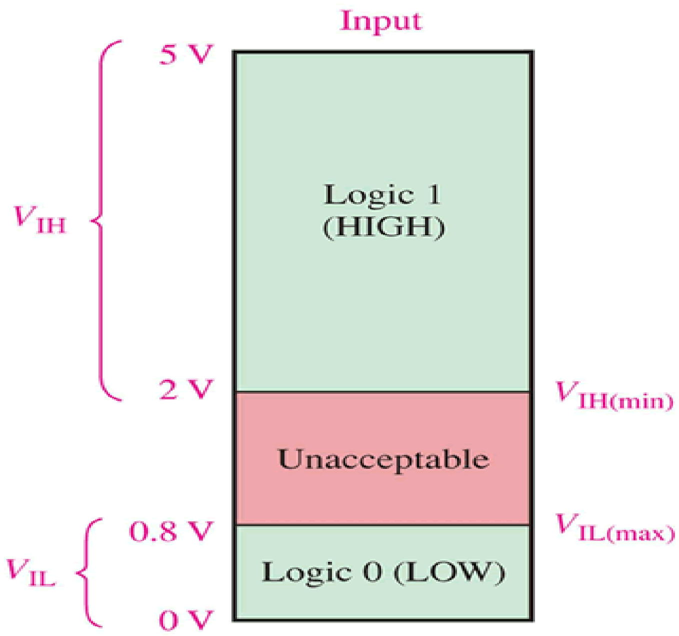
- noise is present in all real systems
- this adds random fluctuations to voltages representing logic levels
- to cope with noise, the voltage ranges defining the logic levels are more tightly constrained at the output of a gate than at the input
- thus small amounts of noise will not affect the circuit
- the maximum noise voltage that can be tolerated by a circuit is termed its **noise immunity** (noise Margin)

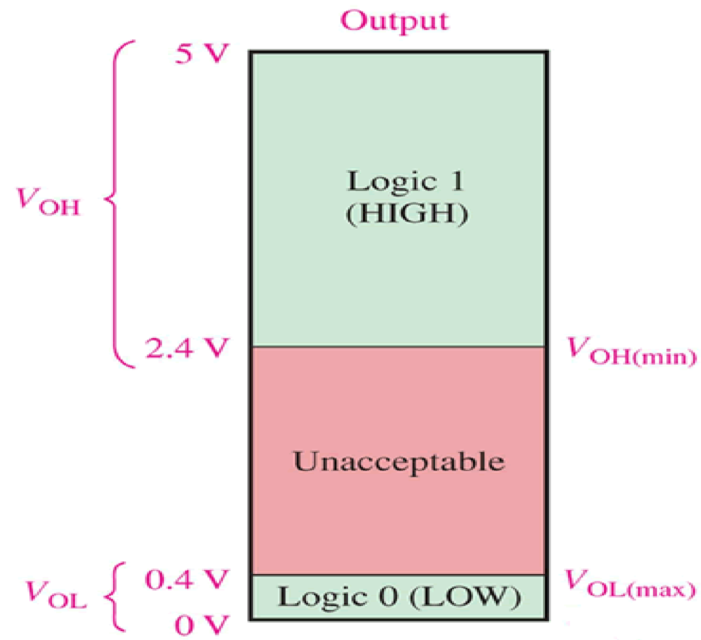


$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$
$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

Digital IC Terminology

Noise Margin





Standard 74XX Series Voltage Levels

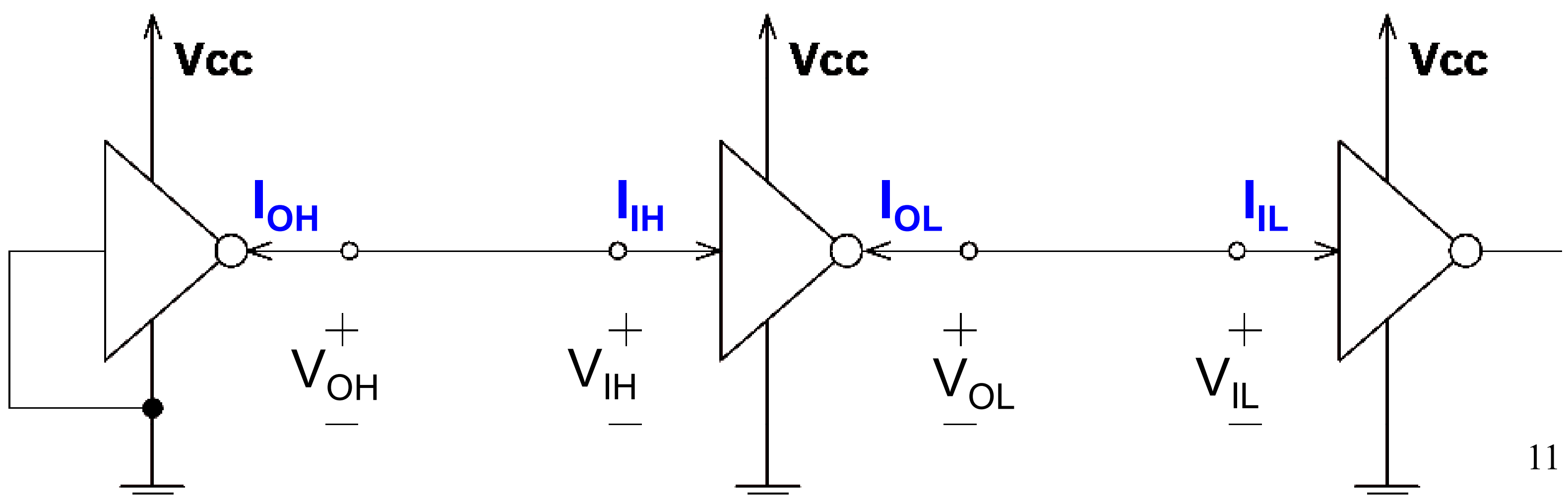
Parameter	Minimum	Typical	Maximum	
V_{OL}		0.2 V	0.4 V	Noise margin
V_{IL}			0.8 V	= 0.4 V
V_{OH}	2.4 V	3.4 V		Noise margin
V_{IH}	2.0 V			= 0.4 V

Noise margin (HIGH) = V_{OH} (min) − V_{IH} (min)
Noise margin (LOW) = V_{IL} (max) − V_{OL} (max)

Digital IC Terminology

Current Parameters:

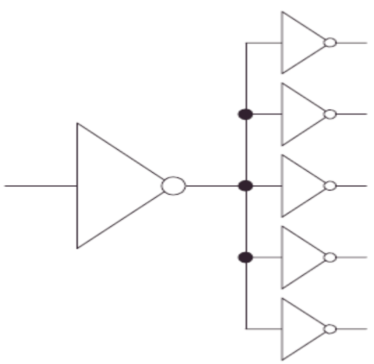
- I_{OH} – Current flowing into an output in the logical "1" state under specified load conditions
- I_{OL} – Current flowing into an output in the logical "0" state under specified load conditions
- I_{IH} – Current flowing into an input when a specified HI level is applied to that input
- I_{IL} – Current flowing into an input when a specified LO level is applied to that input



fanout

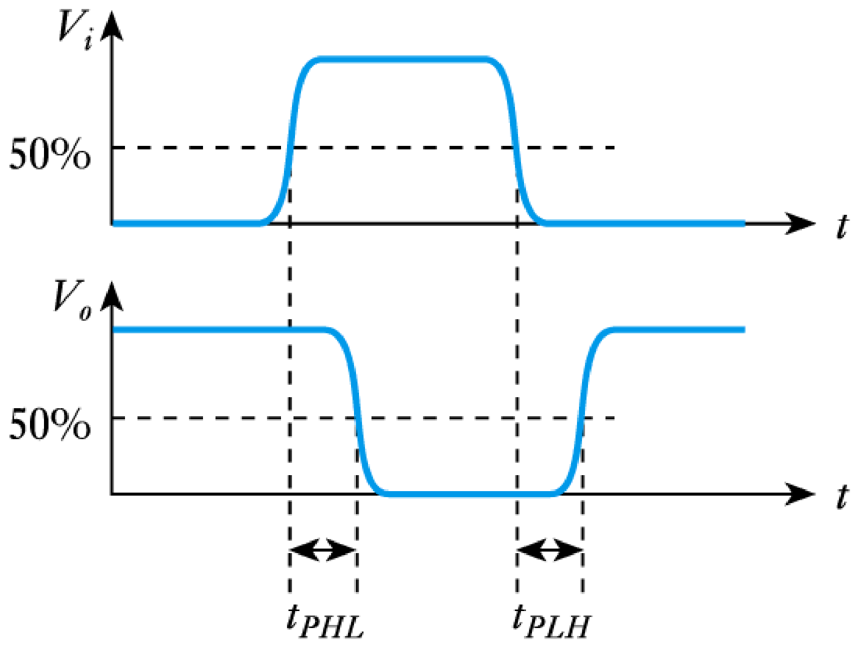
- The maximum number of standard logic inputs that an output can drive reliably.
- Also known as the *loading factor*.
- Related to the current parameters (both in high and low states.)

$$\textbf{DC fanout} = \min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$$



Digital IC Terminology

- **Timing considerations**
  - all gates have a certain **propagation delay time**, t_{PD}
  - this is the average of the two switching times



$$t_{PD} = \frac{1}{2}(t_{PHL} + t_{PLH})$$

Digital IC Terminology

Power Requirements

- Every IC needs a certain amount of electrical power to operate.
- V_{cc} (TTL)
- V_{DD}(MOS)
- Power dissipation determined by I_{cc} and V_{cc}.
- Average $I_{cc}(avg) = (I_{CCH} + I_{CCL})/2$
- $P_D(avg) = I_{cc}(avg) \times V_{cc}$

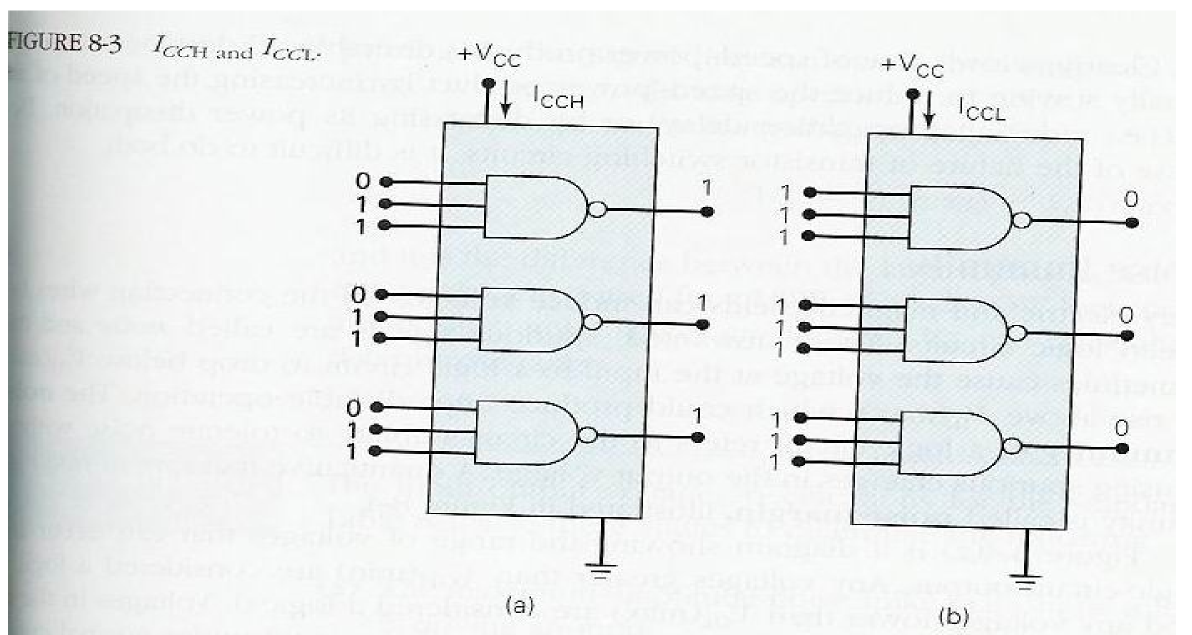


FIGURE 8-3 I_{CCH} and I_{CCL}.

Speed-Power Product

- Desirable properties:
  - Short propagation delays (high speed)
  - Low power dissipation
- Speed-power product measures the combined effect.

Interfacing Logic Families

- We've seen that different logic families have different voltage and current specifications.

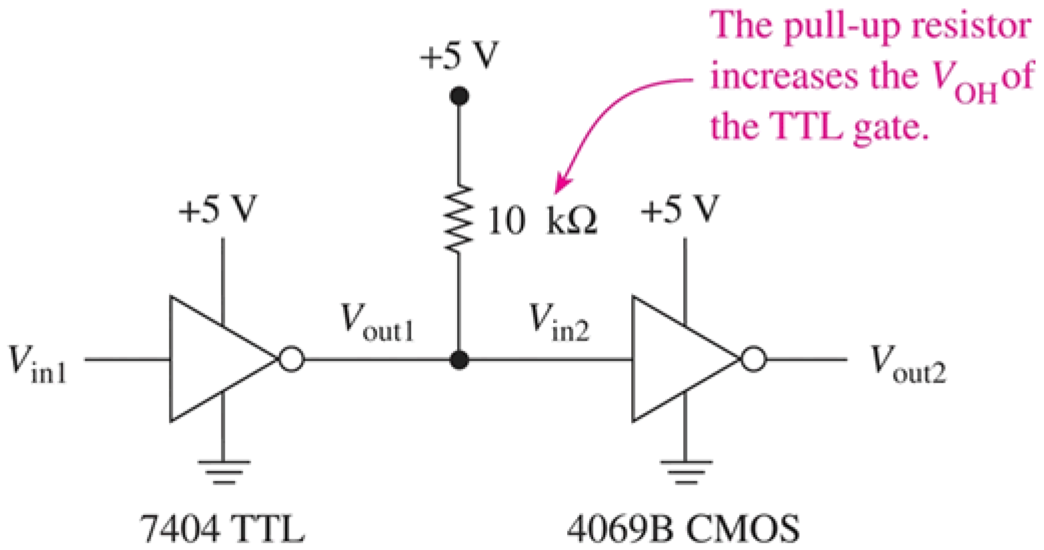
TABLE 9–4 Worst-Case Values for Interfacing Considerations[a]

Parameter	4000B CMOS	74HCMOS	74HCTMOS	74TTL	74LSTTL	74ALSTTL
V_{IH} (min.) (V)	3.33	3.5	2.0	2.0	2.0	2.0
V_{IL} (max.) (V)	1.67	1.0	0.8	0.8	0.8	0.8
V_{OH} (min.) (V)	4.95	4.9	4.9	2.4	2.7	2.7
V_{OL} (max.) (V)	0.05	0.1	0.1	0.4	0.4	0.4
I_{IH} (max.) (μA)	1	1	1	40	20	20
I_{IL} (max.) (μA)	−1	−1	−1	−1600	−400	−100
I_{OH} (max.) (mA)	−0.51	−4	−4	−0.4	−0.4	−0.4
I_{OL} (max.) (mA)	0.51	4	4	16	8	4

[a]All values are for $V_{supply} = 5.0$ V.

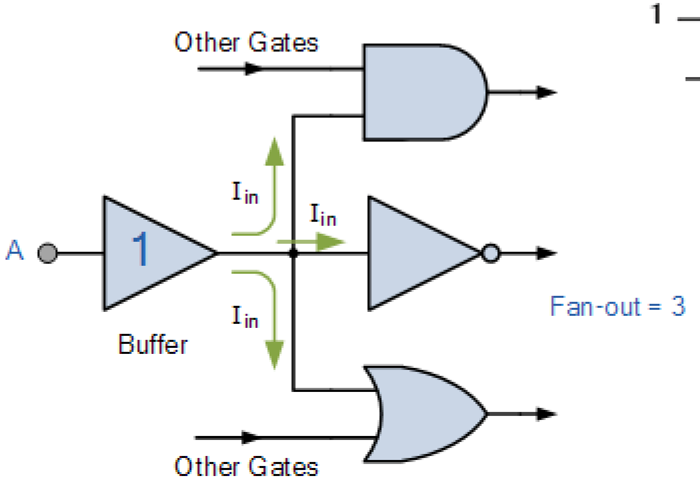
Voltage-Related Interfacing Problems

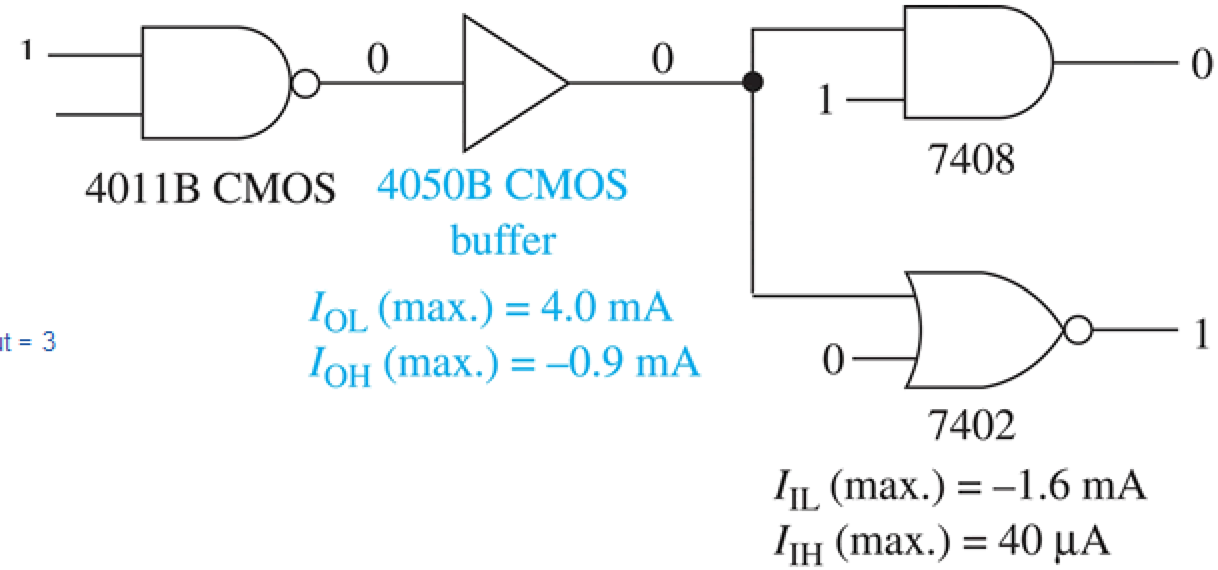
- In some interfacing situations, a HIGH output pin may produce a voltage that is too low to be recognized as a HIGH by the input pin it's connected to.
- The solution in such cases is to use a pull-up resistor
- Example: TTL to CMOS
  - ✓ A TTL HIGH output may be as low as 2.4 V.
  - ✓ But a CMOS input expects HIGHs to be at least 3.33 V.



Current-Related Interfacing Problems

- In some interfacing situations, either a HIGH output pin may not source enough current to drive the input pin it's connected to, or a LOW output pin may not sink enough current to drive the input pin it's connected to.
- The solution in such cases is to use a buffer.
- Example: CMOS to TTL
- A CMOS LOW output can only sink 0.51 mA.
- But as much as 1.6 mA may flow out of a TTL LOW input.
- It can also be used for increasing the fanout

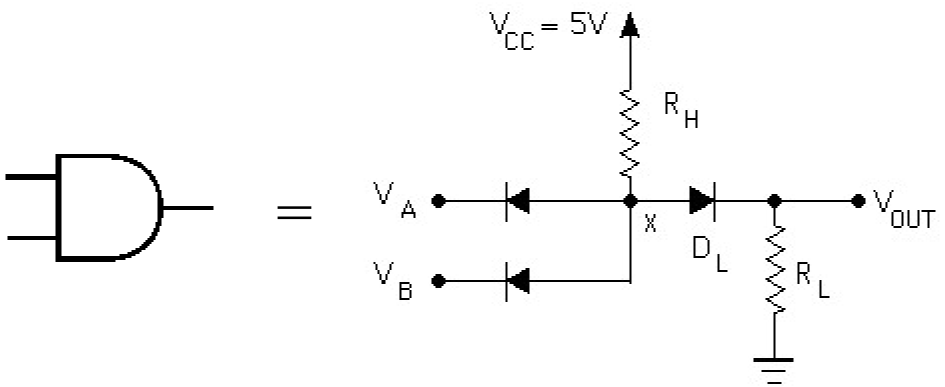




Notes about Families

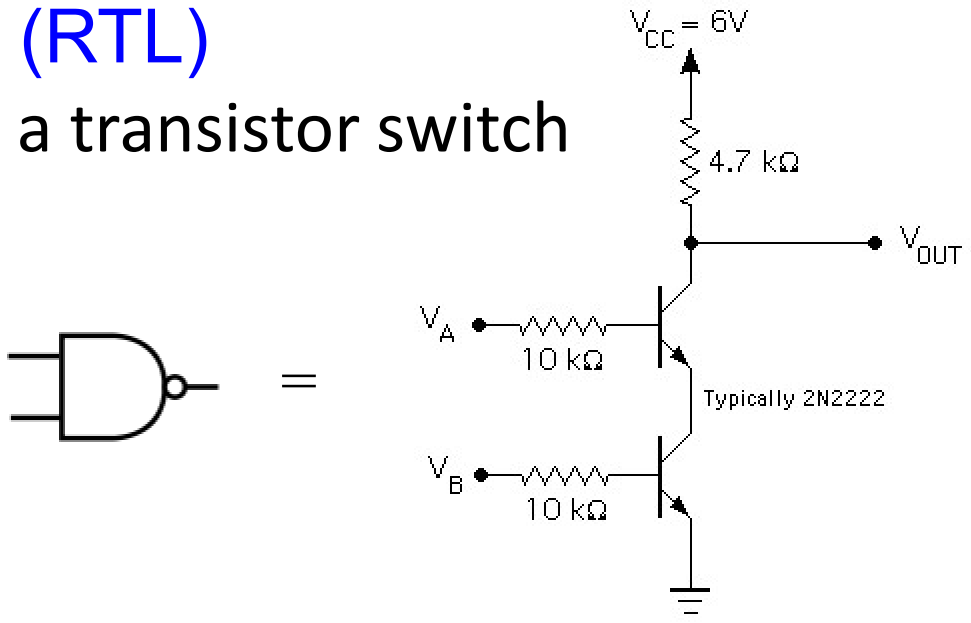
Diode Logic (DL)

- simplest; does not scale
- NOT not possible (need an active element)



Resistor-Transistor Logic (RTL)

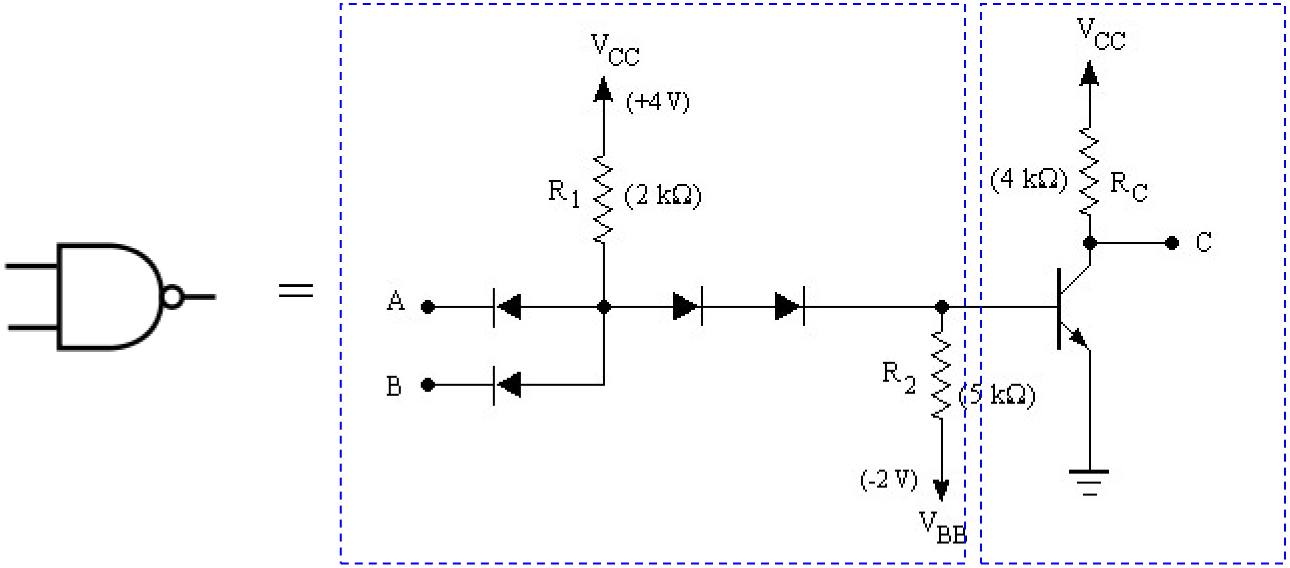
- replace diode switch with a transistor switch
- can be cascaded
- large power draw



Then

Diode-Transistor Logic (DTL)

- essentially diode logic with transistor amplification
- reduced power consumption
- faster than RTL

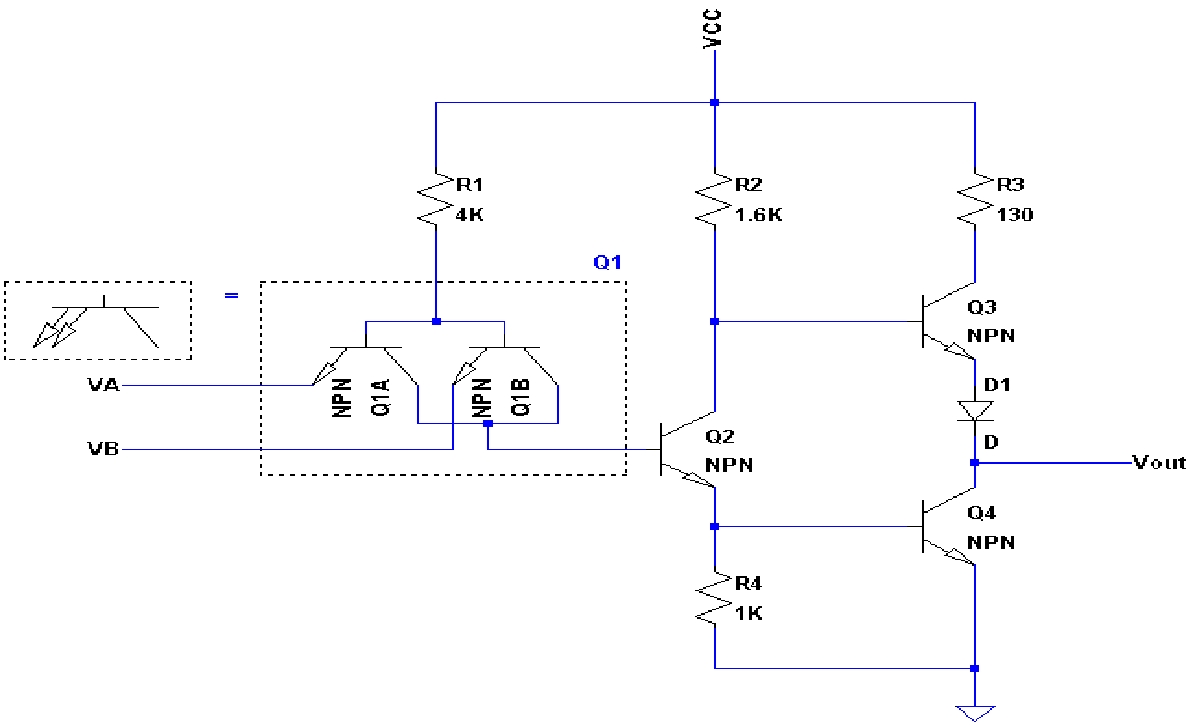


DL AND gate

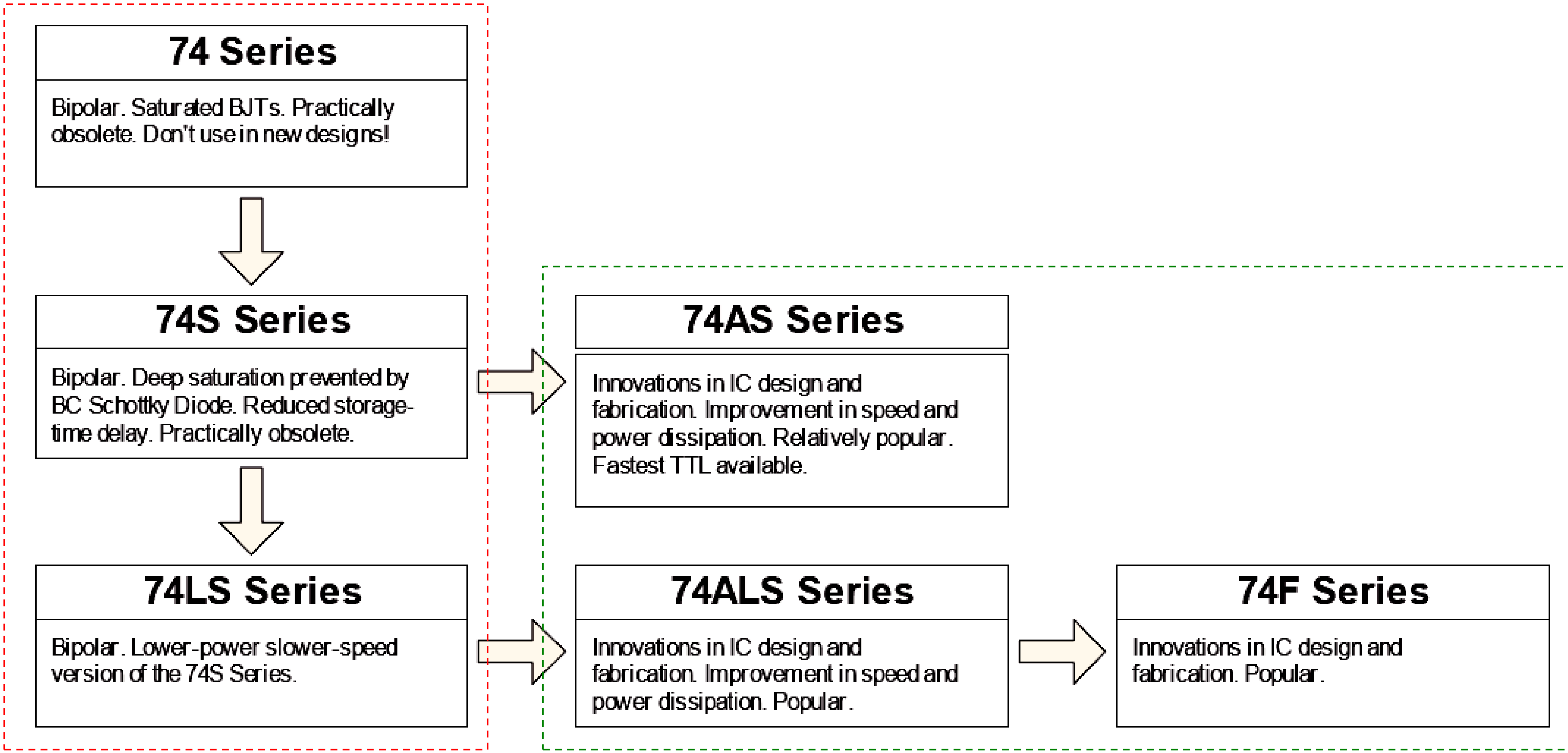
Saturating inverter

TTL Logic Families

- **TTL: Transistor-Transistor Logic**
  - ✓ first introduced by in 1964 (Texas Instruments)
  - ✓ TTL has shaped digital technology in many ways
  - ✓ one of the most widely used families for small- and medium-scale devices – rarely used for VLSI
  - ✓ Standard TTL family (e.g. 7400) is obsolete
  - ✓ Newer TTL fam
  - ✓ High energy cor
  - ✓ relatively insen
  - ✓ Distinct feature:



TTL family evolution



Legacy: don't use in new designs

Widely used today

ECL

Emitter-Coupled Logic (ECL)

- based on BJT, but removes problems of delay time by preventing the transistors from saturating
- very fast operation - propagation delays of 1ns or less
- high power consumption, perhaps 60 mW/gate
- Logic levels. “0”: –1.7V. “1”: –0.8V
- Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families.
- low noise immunity of about 0.2-0.25 V
- used in some high speed specialist applications, but now largely replaced by high speed CMOS

CMOS Complimentary MOS (CMOS)

- Considerably lower energy consumption than TTL and ECL, which has made portable electronics possible.
- most widely used family for large-scale devices
- combines high speed with low power consumption
- usually operates from a single supply of 5 – 15 V
- excellent noise immunity of about 30% of supply voltage
- can be connected to a large number of gates (about 50)

- <u>Things to watch out for</u>:
  – don't leave inputs floating (in TTL these will float to HI, in CMOS you get undefined behaviour)
  – susceptible to electrostatic damage (finger of death)

CMOS/TTL power requirements

- TTL power essentially constant (no frequency dependence)
- CMOS power scales as $\propto f \times C \times V^2$

frequency (f), eff. capacitance (C), supply volt. (V)

- At high frequencies (>> MHz) CMOS dissipates more power than TTL
- Overall advantage is still for CMOS even for very fast chips – only a relatively small portion of complicated circuitry operates at highest frequencies

CMOS family evolution

obsolete

4000 Series

CMOS. Wide supply voltage range. High noise margin. Low speed. Weak output drive. Practically obsolete.

74C Series

CMOS. Pin-compatible with TTL devices. Low speed. Obsolete. Replaced by HC/HCT family.

74HC/HCT Series

CMOS. Drastic increase in speed. Higher output drive capability. HCT input voltage levels compatible with TTL.

74AC/ACT Series

CMOS. Functionally compatible, but not pin-compatible to TTL. Improved noise immunity and speed. ACT inputs are TTL compatible.

74AHC/AHCT Series

CMOS. Improved speed, lower power, lower drive capability.

BiCMOS Logic

CMOS/Bipolar. Combine the best features of CMOS and bipolar. Low power high speed. Bus interfacing applications (74BCT, 74ABT)

74LVC/ALVC/LV/AVC

CMOS. Reduced supply voltage.
LVC: 5V/3.3V translation
ALVC: Fast 3.3V only
AVC: Optimised for 2.5V, down to 1.2V

- Power reduction is one of the keys to progressive growth of integration

Overview

TTL

Logic Family	T_{PD}	$T_{rise/fall}$	$V_{IH,min}$	$V_{IL,max}$	$V_{OH,min}$	$V_{OL,max}$	Noise Margin
74	22ns		2.0V	0.8V	2.4V	0.4V	0.4V
74LS	15ns		2.0V	0.8V	2.7V	0.5V	0.3V
74F	5ns	2.3ns	2.0V	0.8V	2.7V	0.5V	0.3V
74AS	4.5ns	1.5ns	2.0V	0.8V	2.7V	0.5V	0.3V
74ALS	11ns	2.3ns	2.0V	0.8V	2.5V	0.5V	0.3V
ECL	1.45ns	0.35ns	-1.165V	-1.475V	-1.025V	-1.610V	0.135V
4000	250ns	90ns	3.5V	1.5V	4.95V	0.05V	1.45V
74C	90ns		3.5V	1.5V	4.5V	0.5V	1V
74HC	18ns	3.6ns	3.5V	1.0V	4.9V	0.1V	0.9V
74HCT	23ns	3.9ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AC	9ns	1.5ns	3.5V	1.5V	4.9V	0.1V	1.4V
74ACT	9ns	1.5ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AHC	3.7ns		3.85V	1.65V	4.4V	0.44V	0.55V

CMOS

- Values typical for V_{cc}/V_{dd} = 5V
- When interfacing different families, pay attention to their input/output voltage, current (fanout) specs

Some Gates

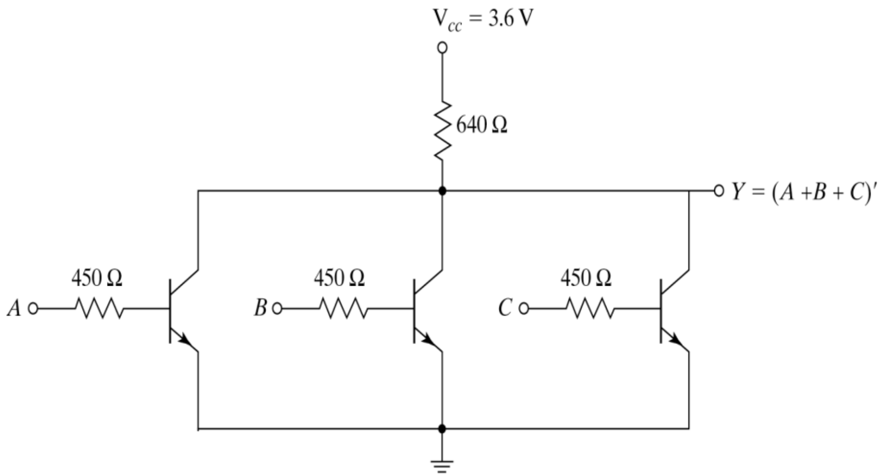


Fig. 10-8 RTL Basic NOR Gate

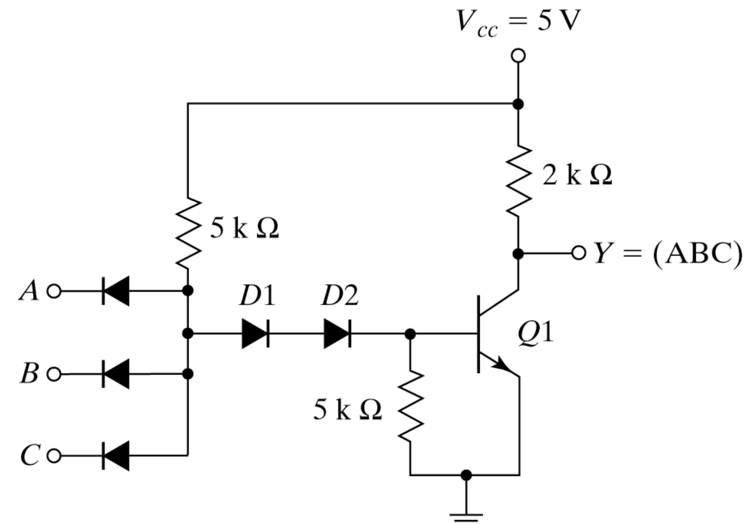
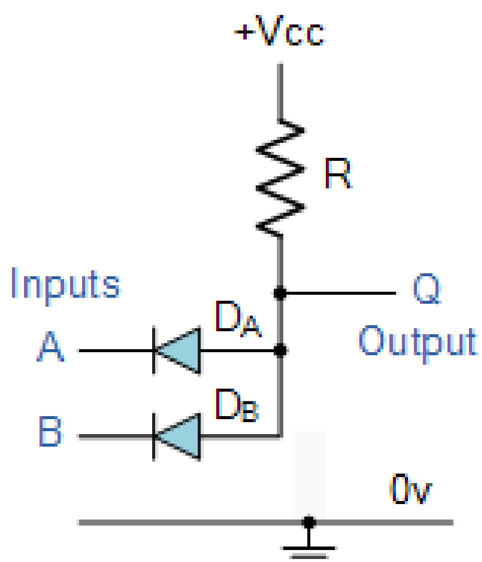


Fig. 10-9 DTL Basic NAND Gate



2-input AND Gate
Diode-Resistor Logic

Some Gates

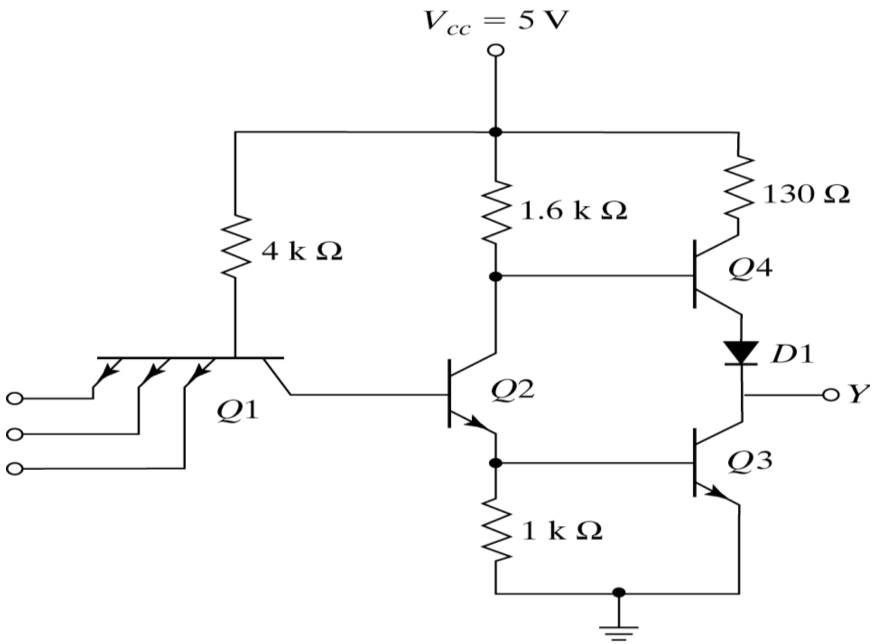
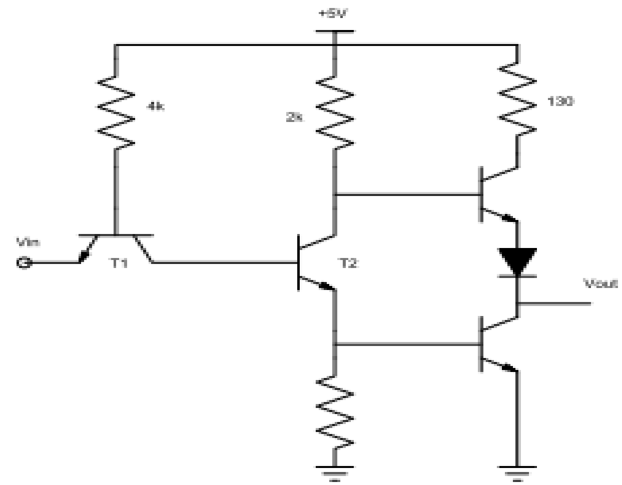
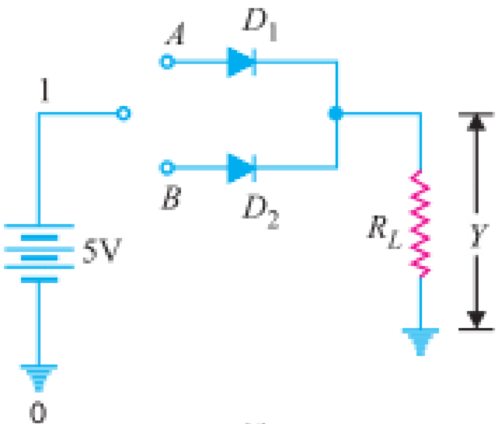


Fig. 10-14 TTL Gate with Totem-Pole Output

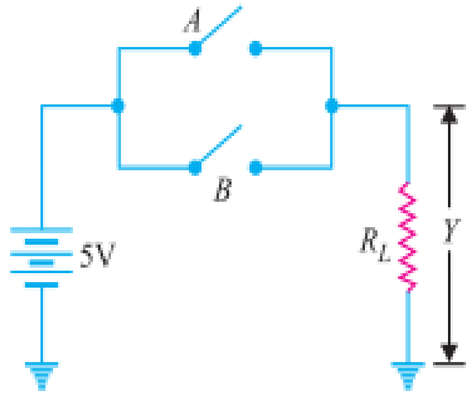


7400 Series of TTL Inverters

Diode-Resistor OR gate



(*i*)



(*ii*)

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

(*iii*)

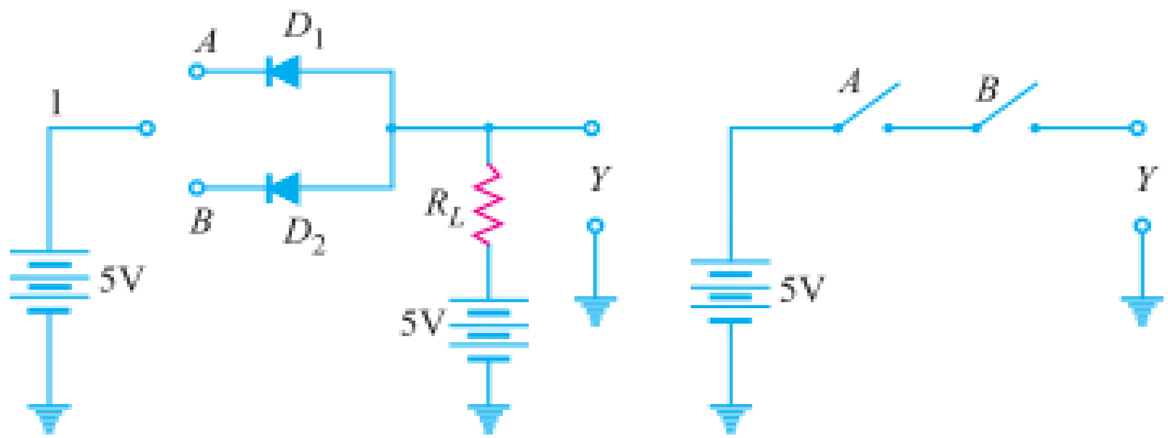
(*i*) When both *A* and *B* are connected to ground, both diodes are non-conducting. Hence, the output voltage is ideally zero (low voltage). In terms of binary, when $A = 0$ and $B = 0$, then $Y = 0$ as shown in the truth table in Fig. 26.6 (*iii*).

(*ii*) When *A* is connected to ground and *B* connected to the positive terminal of the battery, diode D_2 is forward biased and diode D_1 is non-conducting. Therefore, diode D_2 conducts and the output voltage is ideally +5 V. In terms of binary, when $A = 0$ and $B = 1$, then $Y = 1$ [See Fig. 26.6 (*iii*)].

(*iii*) When *A* is connected to the positive terminal of the battery and *B* to the ground, diode D_1 is on and diode D_2 is off. Again the output voltage is +5 V. In binary terms, when $A = 1$ and $B = 0$, then $Y = 1$ [See Fig. 26.6 (*iii*)].

(*iv*) When both *A* and *B* are connected to the positive terminal of the battery, both diodes are on. Since the diodes are in parallel, the output voltage is +5 V. In binary terms, when $A = 1$ and $B = 1$, then $Y = 1$ [See Fig. 26.6 (*iii*)].

Diode-Resistor AND gate



(i) (ii)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(iii)

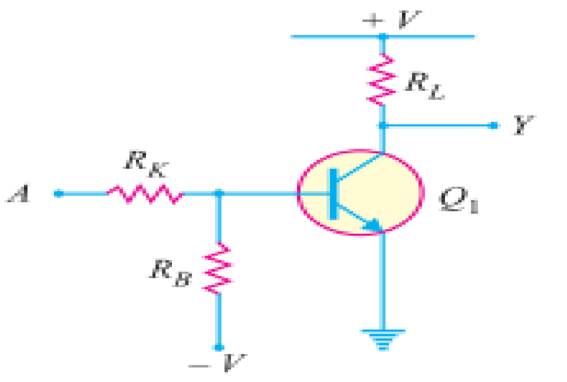
(i) When both A and B are connected to ground, both the diodes (D_1 and D_2) are forward biased and hence they conduct current. Consequently, the two diodes are grounded and output voltage is zero. In terms of binary, when $A = 0$ and $B = 0$, then $Y = 0$ as shown in truth table in Fig. 26.8 (*iii*).

(ii) When A is connected to the ground and B connected to the positive terminal of the battery, diode D_1 is forward biased while diode D_2 will not conduct. Therefore, diode D_1 conducts and is grounded. Again output voltage will be zero. In binary terms, when $A = 0$ and $B = 1$, then $Y = 0$. This fact is shown in the truth table.

(iii) When B is connected to the ground and A connected to the positive terminal of the battery, the roles of diodes are interchanged. Now diode D_2 will conduct while diode D_1 does not conduct. As a result, diode D_2 is grounded and again output voltage is zero. In binary terms, when $A = 1$ and $B = 0$, then $Y = 0$. This fact is indicated in the truth table.

(iv) When both A and B are connected to the positive terminal of the battery, both the diodes do not conduct. Now, the output voltage is +5 V because there is no current through R_L.

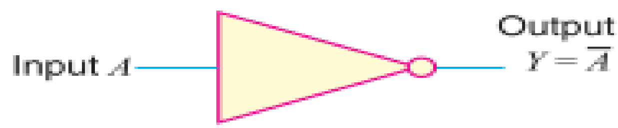
NOT gate



(i)

A	Y
0	1
1	0

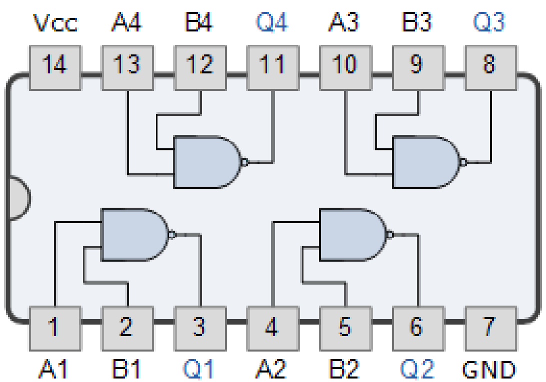
(ii)



(iii)

Figure 26.10 (*i*) shows a *typical inverter circuit. When A is connected to ground, the base of transistor Q_1 will become negative. This negative potential causes the transistor to cut off and collector current is zero and output is + V volts. In binary terms, when $A = 0$, $Y = 1$. If sufficiently large positive voltage is applied at A, the base of the transistor will become positive, causing the transistor to conduct heavily. Therefore, the output voltage is zero. In binary terms, when $A = 1$, $Y = 0$. Fig.

Common ICs



7400 Quad 2-input Logic NAND Gate

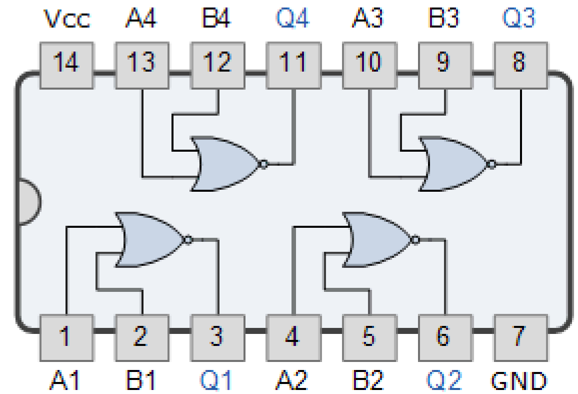
Also:

74LS00 Quad 2-input

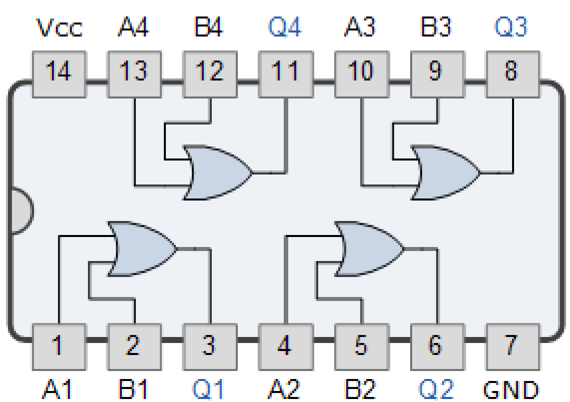
74LS10 Triple 3-input

74LS20 Dual 4-input

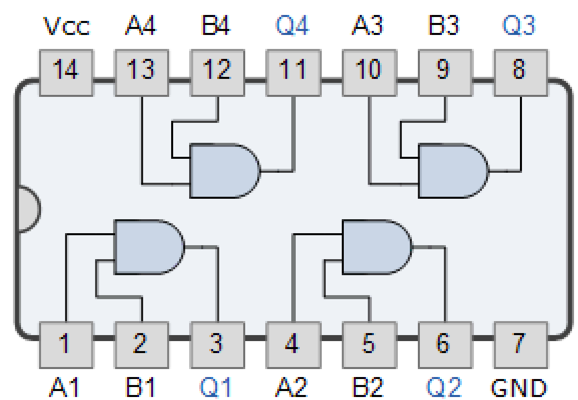
74LS30 Single 8-input



7402 Quad 2-input NOR Gate



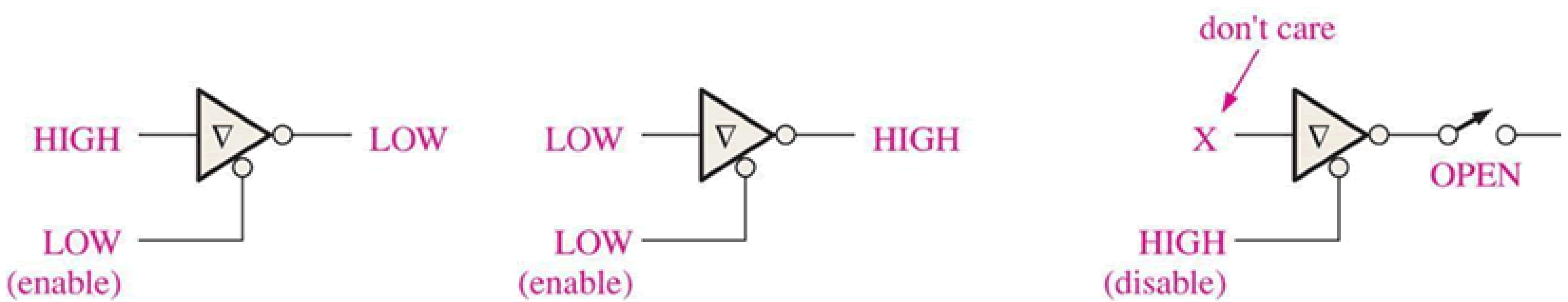
7432 Quad 2-input Logic OR Gate



7408 Quad 2-input AND Gate

Three-State Output (also called tri-state output)

- In addition to the two usual output states (HIGH and LOW), has a third output state called high-impedance ("high-Z").
- In the high-Z state, the output is disconnected from the external circuit.
- Useful when the outputs of many chips are tied to the same bus: at any time, only one of them should be connected to the bus.



(a) Enabled for normal logic operation

(b) High-Z state